

Please add the following new claims:

02 1 28. A wafer dividing method comprising the steps of:
2 forming grooves in a surface of a wafer, on which surface semiconductor
3 elements are formed, along dicing lines, said grooves being deeper than a
4 thickness of a finished chip;
5 attaching a holding member on said surface of the wafer on which the
6 semiconductor elements are formed; and
7 lapping and polishing a bottom surface of the wafer to said thickness of the
8 finished chip, thereby dividing the wafer into chips,
9 wherein in the step of dividing the wafer into the chips, the lapping and polishing
10 is continued until the thickness of the wafer becomes equal to the
11 thickness of the finished chip, even after the wafer has been divided into
12 the chips by the lapping and polishing.

1 29. The wafer dividing method according to claim 28 wherein a depth of each
2 groove is greater than the thickness of the finished chip by at least 5 μm .

1 30. The wafer dividing method according to claim 28 wherein said holding
2 member comprises a substrate coated with an adhesive material.

1 31. A method of manufacturing a semiconductor device, comprising the steps
2 of:
3 forming semiconductor elements in a major surface of a wafer;
4 forming grooves in said major surface of the wafer along dicing lines, said
5 grooves being deeper than a thickness of a finished chip;
6 attaching an adhesive sheet on said major surface of the wafer;
7 lapping and polishing a bottom surface of the wafer to said thickness of the
8 finished chip, thereby dividing the wafer into chips; and
9 separating each of the divided chips from the adhesive sheet and sealing said
10 each chip in a package,
11 wherein in the step of dividing the wafer into the chips, the lapping and polishing
12 is continued until the thickness of the wafer becomes equal to the
13 thickness of the finished chip, even after the wafer has been divided into
the chips by the lapping and polishing.

1 32. The method of manufacturing a semiconductor device, according to claim
2 31, wherein a depth of each groove is greater than the thickness of the finished chip by
3 at least 5 μm .